REMARKS

In response to the final Official Action of December 12, 2008, claims 24, 30, 31, 41, 42, 45, and 58 have been amended in a manner which is believed to particularly point out and distinctly claim the invention. Minor amendment has also been made to claims 27 and 33. Claims 28 and 29 are canceled as a result of the amendment to claim 24.

Applicant's attorney would like to thank Examiners Campos and Shah for their helpful comments made during a telephone interview with the undersigned attorney on February 17, 2009. At that time, discussion was had concerning independent claim 24, including proposed usage of the term "configured to" and specifying that the first terminals and second terminals each contain a data port and that at least one of the first terminals and the second terminals also comprises a control port and an address port. Support for the amendment to the claims is found in the original application as filed, including Figures 2-5 and the specification at page 10, line 18 through page 13, line 8.

Minor amendment has been made to the specification at page 11 to correct typographical errors and to reference Figure 1. No new matter is added.

Claim Rejections - 35 USC §103

At section 3, claims 24, 28-43, and 45-58 are rejected under 35 USC §103(a) as unpatentable in view of US patent 6,167,487, Camacho, et al (hereinafter Camacho) in view of US patent 6,826,657, Ware, et al (hereinafter Ware).

With respect to claim 24, the Office states that Camacho discloses at least two memory areas for storing data with the parenthetical observation that the word "for" is interpreted as intended use. Based upon the telephonic interview with the undersigned attorney on February 17, 2009, it was agreed that the term "configured to" does not connote an intended use and claim 24 is amended to reflect this change in term usage with regard to the memory areas and first and second terminals.

With regard to the reliance of Camacho and Ware, applicant's attorney discussed the arguments previously presented with regard to both Camacho and Ware. In particular, applicant agrees with the Office that Camacho does not expressly disclose that in the case of sole addressing, the data is provided within all of the at least two memory areas through

data ports of both terminals. Applicant does not agree with the Office that Ware discloses this feature.

In particular, it is respectfully submitted that in the case of sole addressing and accessing data, the access controllers provide access to all of the at least two memory areas by a respective control port and address port of only one of the first terminals and second terminals and provide the data within all of the at least two memory areas through data ports of both the first terminals and second terminals. As amended, claim 24 specifies the features that both the first terminals and second terminals each have a data port and that at least one of the first terminals and the second terminals also comprises a control port and an address port.

In response to the Office's reliance upon Ware and in particular Figure 6A thereof, Figure 6A of Ware is below provided with additional reference signs QDx, and QDy.

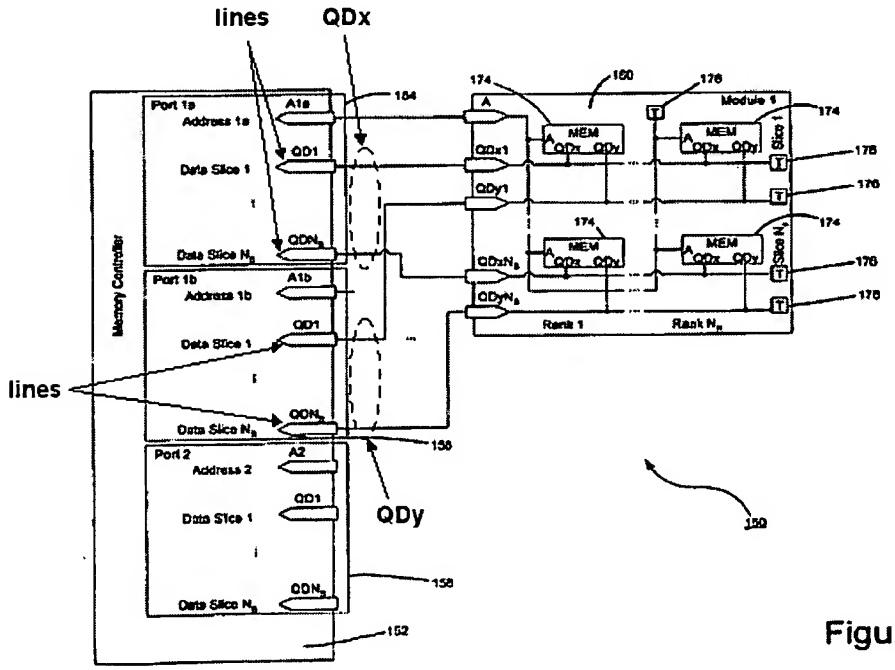


Figure 6A

As can be seen from Figure 6A of Ware, a first port 1a and a second port 1b are provided which correspond to the first terminals and second terminals according to the present invention. Furthermore, each of these ports 1a and 1b is connected to memory components 174 of a memory 160. Ware discloses explicitly that "*each memory*

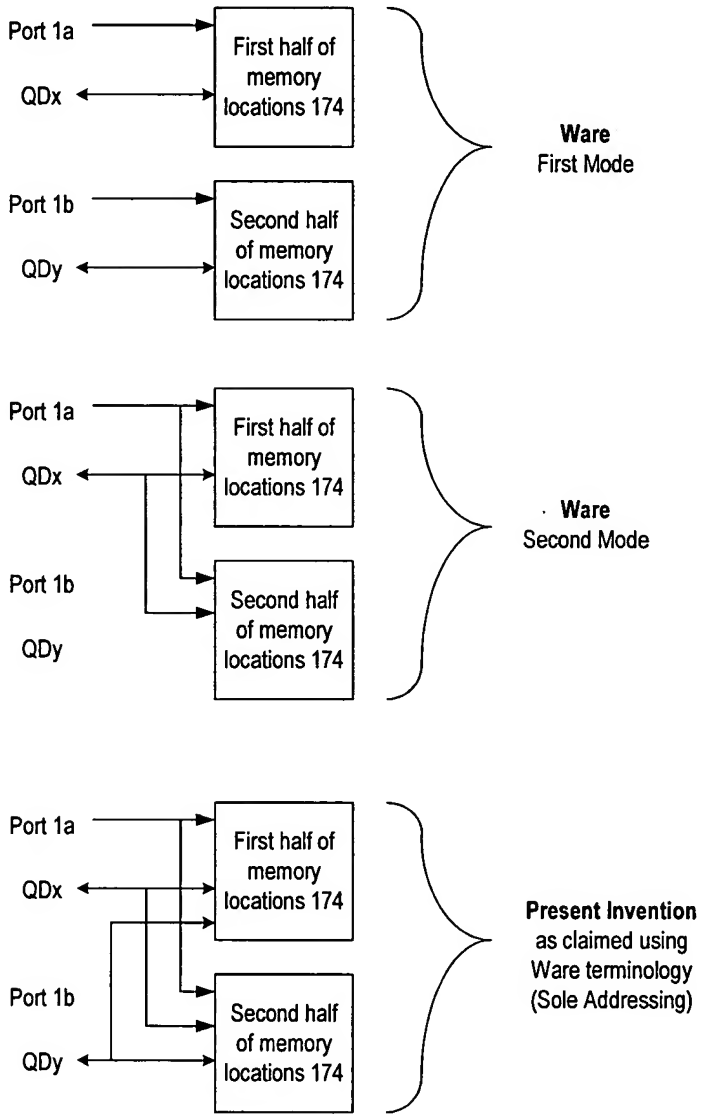
component (MEM) has two data bus ports denoted QDx and QDy" (Ware: col. 15, l. 13-14). In other words, according to Ware, only two data buses are provided for connecting ports 1a and 1b to the memory components 174, wherein a data bus corresponds to the data port of the first or second terminals according to the present invention. More particularly, Ware explicitly teaches that QDx or QDy each denotes merely one data bus (Ware: col. 15, l. 22-23: "...*QDx data bus, and the QDy data bus...*"). In support, both data buses are denoted by QDx or QDy in Figure 6A. In general, a bus, in particular a parallel bus, comprises several parallel lines, ports or pins. According to Ware, each data bus QDx or QDy comprises N_S lines, ports or pins. By way of example, if the number of lines is 16, it may be possible to process 16 bits in parallel. However, it is still only one bus having 16 parallel lines or ports. In Figure 6A, only the first line QD1 and the last line QDN_S of the data bus QDx and QDy respectively are depicted, while the further lines are indicated by dots. Hence, the two data buses QDx and QDy are the only data buses having N_S lines according to Ware.

Furthermore, the data bus QDx is configured to only connect port 1a to the memory components 174 while data bus QDy is configured to only connect port 1b to the memory components 174 (Ware: col. 15, l. 13-23; Fig. 6a, 6b). In addition, Ware discloses that access to the memory module 160 may be done in a first mode. Within the first mode, half of the storage locations in the memory components 174 are accessible through the QDx data bus and the other half of the storage locations in the memory components 174 is accessible through the QDy data bus (Ware: col. 15, l. 20-23, Fig. 6a). Thus, in the first mode, one data bus provides access to half of the memory locations in the memory components 174 and the other data bus provides access to the other half of the memory locations in the memory components 174.

Further, there is a second mode according to Ware, within which all of the storage locations of the memory components 174 are accessible through the QDx data bus, while the QDy data bus is unused (Ware: col. 15, l. 20-23).

Such a technique as disclosed by Ware is unlike the present invention as claimed. In short, Ware provides that one data bus (QDx) can, when in the second mode, access data from all memory locations of memory components 174. Ware does not disclose or suggest that one data bus (e.g., QDx) can be combined with another data bus (e.g., QDy)

to access all memory locations of memory components 174 while the addressing of the memory locations is performed solely by the address lines associated with one terminal (e.g., Port la). The following diagrams make this distinction clear:



According to the subject matter of amended claim 24, it is explicitly taught that "access controllers provide access to all of the at least two memory areas by a respective control port and address port of only one of the first terminals and second terminals and provide the data within all of the at least two memory areas through data ports of both the first terminals and second terminals." The only buses according to Ware used by both

ports 1a and 1b are data bus QDx and data bus QDy. Even if QD1 and QDN_S were understood to be two buses (which applicant does not subscribe to), and not two lines as asserted by the applicant, both QD1 and QDN_S are always and compulsorily used by the same port 1a (i.e. first terminal). It is excluded by the disclosure of Ware that QD1 or QDN_S is used by the other port 1b (i.e. second terminal). Thus, it is not possible to read the apparatus according to Ware under the present wording of amended claim 24. According to claim 24, two conditions must be fulfilled at the same time. The first condition is that a first data port and a second data port respectively can be used by first terminals and second terminals. The second condition is that both data ports can be also used by only the first terminals or only the second terminals. These conditions are not fulfilled according to Ware, regardless of whether QD1 and QDN_S are understood to be two data buses, which applicant understands otherwise.

Indeed, Ware discloses maximizing memory bandwidth across the full memory address space (Ware: col. 32 l. 61 – col. 33, l. 6). However, compared to the present invention, the bandwidth according to Ware is limited. It is not possible to use both the data bus of the first terminal and the data bus of the second terminal at the same time by using only a control port and address port of <u>one</u> of the terminals. Hence, the provided bandwidth in case of sole addressing according to Ware is half of the provided bandwidth according to the present application, since according to the present invention both data ports (buses) can be used at the same time by a control port and address port of only <u>one</u> terminal. In other words, the bandwidth is significantly increased by the apparatus according to the present application.

Consequently, *Ware* does not disclose "wherein in case of sole addressing and accessing the data, the access controllers provide access to all of the at least two memory areas by a respective control port and address port of only one of the first terminals and second terminals and provide the data within all of the at least two memory areas through data ports of both the first terminals and second terminals," as recited in amended claim 24. Thus, *Camacho* in view of *Ware* fails to render claim 24 obvious, and therefore applicant respectfully requests allowance of claim 24.

Claims 41-42, 45 and 58 are independent claims which contain similar features as claim 24 described above. For at least the reasons presented above regarding claim 24,

claims 41-42, 45 and 58 are also patentable over *Camacho* in view of *Ware*. Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 41-42, 45 and 58.

Claims 25-27, 30-40, 43-44 and 46-57 are dependent claims and recite additional features not recited in the independent claims. All of the dependent claims are also allowable at least in view of this dependency.

Claims 28 and 29 have been canceled in view of the amendment to claim 24.

In view of the foregoing, it is respectfully submitted that the present application as amended is in condition for allowance and such action is earnestly solicited.

Respectfully submitted,

Dated: March 10, 2009

Alfred A. Fressola
Attorney for Applicants
Registration No. 27,550

WARE, FRESSOLA, VAN DER
SLUYS & ADOLPHSON LLP
Building Five, Bradford Green
755 Main Street, P.O. Box 224
Monroe, CT 06468
Telephone: (203) 261-1234
Facsimile: (203) 261-5676
USPTO Customer No. 004955